UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/387,857	09/01/99	SUGAYA	F 1776/00039

MM91/0911

POLLOCK VANDE SANDE & PRIDDY
P O BOX 19088
WASHINGTON DC 20036-3425

EXAMINER	
NOVACEK,C	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED:
09/11/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/387,857	SUGAYA, FUMITAKA	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- Th MAILING DATE of this communication appears on th cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/059,590* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the communication filed September 1, 1999.

Drawings

The drawings are objected to because in Fig. 1A reference element "1" points to the same object as "2". In Fig. 10A, reference element "31" points to the same object as "32". Correction is required.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The disclosure is objected to because of the following informalities:

The first sentence of the specification should be updated to read, "This application is a divisional of Application Serial No. 09/059,590, now U.S. Patent No., 6,288,423."

The phrase "opposing the second conductive film to the first conductive film through the dielectric film" is not understood by the Examiner. This phrase occurs on pg. 7, lines 14-15, pg. 8, lines 7-8 and 23-25, pg. 9, lines 15-17, pg. 10, lines 10-11 of the specification.

In the phrase, "leaving the first conductive film behind on a bottom", it is not apparent what the first conductive film is left on the bottom of.

Appropriate correction is required.

Claim Objections

Claim 32 is objected to because of the following informalities: Lines 8-9 of claim 32 recite the limitation of "said second substrate". This limitation lacks antecedent basis in claim. This is believed to be a typographical error. The word "second" should be replaced with "semiconductor" to be in accordance with the rest of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 18 of claim 28 and line 22 of claim 32, the phrase "on a bottom" is indefinite because it is not apparent what the first conductive film is left on the bottom of.

In lines 23-25 of claim 28, lines 26-28 of claim 32 and lines 16-18 of claim 36, the meaning of the word "opposing" is unclear. Specifically, it is not understood how the second conductive film is opposed through the dielectric film.

In lines 5-6 of claim 36, the limitation of "forming a mask pattern having two types of openings" is indefinite. It is not clear if this phrase intends to convey that the two openings are different from each other or, if they are different, how they are different from each other (i.e., are they formed by different processes, do they have different shapes, etc.).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1. Claims 32-34, 36, and 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Schoenfeld et al.

In reference to claim 32, Schoenfeld discloses forming an element active region and an element isolation structure (104) on a semiconductor substrate (102) (Fig. 1; col. 4, ln. 19-23). A gate insulating film (106) and a gate electrode (116) are formed in the active region and an impurity is doped into the substrate to form a pair of impurity diffusion layers (108/110) in the surface of the substrate on two sides of the gate electrode (Fig. 1; col. 4, ln. 23-31). A first conductive film (128) is electrically connected to one of the impurity diffusion layers (col. 4, ln. 55-58). A mask pattern (130) having first (142) and second (140) openings is formed on the first conductive film and the mask is used to divide the first conductive film in the first opening while simultaneously forming a recess in the second opening in which the first conductive film is left on the bottom of the recess (Fig. 2-3; col. 4, ln. 61-col. 5, ln. 15). A dielectric film (134) covers the surface of the first conductive film and a second conductive film (136) covers the dielectric film (Fig. 4; col. 5, ln. 16-21).

In reference to claim 33, an insulating interlayer (126) is formed on the entire surface of the substrate and a hole is formed in the interlayer in which one of the impurity diffusion layers

is exposed (Fig. 1; col. 4, ln. 51-55). The first conductive film is formed on the insulating interlayer and in the hole (col. 4, ln. 55-58). The first conductive film is then etched in the first opening until the insulating interlayer is exposed in the first opening (Fig. 3).

In reference to claim 34, Schoenfeld discloses that "The areas of the apertures 140 should be less than the area of the boundary openings 142 in the mask 130". This statement encompasses the situation in which the first opening is not less than twice the width of the second opening (140). Furthermore, Fig. 2 clearly shows the width of the first openings (142) to be significantly more than twice the width of the second openings (140).

In reference to claim 36, a first conductive film (128) is formed in an insulating film region (126) on a semiconductor substrate (102) (Fig. 1). A mask pattern (130) having two different types of openings (140/142) is formed on the first conductive film and the mask is used to divide the first conductive film while it is conformed to a shape of one of the openings (142) and at least one recess is simultaneously formed while the surface of the conductive film is conformed to the shape of the other opening (Fig. 2-3; col. 4, ln. 61-col. 5, ln. 15). An insulating film (134) covers the surface of the first conductive film and a second conductive film (136) covers the insulating film.

In reference to claim 42, Schoenfeld discloses forming an element active region and an element isolation structure (104) on a semiconductor substrate (102) (Fig. 1; col. 4, ln. 19-23). A gate oxide film (106) and a gate electrode (116) are formed in the active region and an impurity is doped into the substrate in the active region to form a pair of impurity diffusion layers (108/110) in the surface of the substrate on two sides of the gate electrode (Fig. 1; col. 4, ln. 23-31). A first conductive film (128) is electrically connected to one of the impurity diffusion layers (col. 4, ln. 55-58). A mask pattern (130) having first (142) and second (142) openings is

formed on the first conductive film and the mask is used to divide the first conductive film below the first opening while simultaneously forming a hole through the first conductive film below the second opening (Fig. 2-3; col. 4, ln. 61-col. 5, ln. 15). A dielectric film (134) covers the surface of the first conductive film and a second conductive film (136) covers the dielectric film (Fig. 4; col. 5, ln. 16-21).

In reference to claim 43, an insulating interlayer (126) is formed on the entire surface of the substrate and a hole is formed in the interlayer in which one of the impurity diffusion layers is exposed (Fig. 1; col. 4, ln. 51-55). The first conductive film is formed on the insulating interlayer and in the hole (col. 4, ln. 55-58). The first conductive film is then etched until the insulating interlayer is exposed in the first and second openings (Fig. 3).

2. Claims 36-38 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Tseng.

In reference to claim 36, Tseng discloses forming a first conductive film (11a) in an insulating film region (9/2) on a semiconductor substrate (1) (Fig. 2; col. 4, ln. 42-62). A mask pattern (15) having two openings (one on each side of the mask shown in Fig. 6) is formed on the first conductive film and the mask is used to divide the first conductive film while it is conformed to a shape of one of the openings and at least one recess is simultaneously formed while the surface of the conductive film is conformed to the shape of the other opening (Fig. 7; col. 5, ln. 30-48). An insulating film (16) covers the surface of the first conductive film and a second conductive film (17) covers the insulating film (Fig. 8; col. 5, ln. 50-67).

In reference to claim 37, the recess (on either side of first conductive layer 11a) reaches the insulating film region (9/2) and, thus exposes the insulating film region (Fig. 7).

In reference to claim 38, Tseng discloses forming an element active region and an element isolation structure (2) on a semiconductor substrate (1) (Fig. 1). An insulating film (9) is

formed on the substrate in the active region and a first conductive film (11a) is formed on the insulating film and the isolation structure (Fig. 2; col. 4, ln. 42-62). A mask pattern (15) having first and second openings (one on each side of the mask pattern shown in Fig. 6) is formed on the first conductive film . The first conductive film is etched using the mask, wherein the conductive film is divided below the first opening while simultaneously forming a hole extending through the conductive film below the second opening (Fig. 7; col. 5, ln. 30-48). A dielectric film (16) covers the first conductive film and a second conductive film (17) is formed on the dielectric film (Fig. 8; col. 5, ln. 50-67).

In reference to claim 40, after the first conductive film (11a) is deposited, it is planarized by polishing prior to deposition of the mask pattern (15) (col. 4, ln. 59-62).

3. Claims 36-39 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwamatsu et al.

In reference to claim 36, Iwamatsu discloses forming a first conductive film (12) in an insulating film region (11/16) on a semiconductor substrate (1) (Fig. 7; col. 15, ln. 58-col. 16, ln. 18). A mask pattern (21) having two openings (one on each side of the mask shown in Fig. 7) is formed on the first conductive film and the mask is used to divide the first conductive film while it is conformed to a shape of one of the openings and at least one recess is simultaneously formed while the surface of the conductive film is conformed to the shape of the other opening (Fig. 8; col. 16, ln. 19-29). An insulating film (17b) covers the surface of the first conductive film and a second conductive film (24) covers the insulating film (Fig. 10-11; col. 16, ln. 36-52).

In reference to claim 37, the recess (on either side of first conductive layer 12) reaches the insulating film region (11/16) and, thus exposes the insulating film region (Fig. 8).

In reference to claim 38, Iwamatsu discloses forming an element active region and an element isolation structure (16) on a semiconductor substrate (1) (Fig. 3). An insulating film (11) is formed on the substrate in the active region and a first conductive film (12) is formed on the insulating film and the isolation structure (Fig. 7; col. 15, ln. 58-col. 16, ln. 18). A mask pattern (21) having first and second openings (one on each side of the mask pattern shown in Fig. 7) is formed on the first conductive film . The first conductive film is etched using the mask, wherein the conductive film is divided below the first opening while simultaneously forming a hole extending through the conductive film below the second opening (Fig. 8; col. 16, ln. 19-29). A dielectric film (17b) covers the first conductive film and a second conductive film (24) is formed on the dielectric film (Fig. 11; col. 16, ln. 36-52).

In reference to claim 39, after the step of forming the second conductive film, impurities are doped into the substrate in the active region to form impurity diffusion layers (8/10) in the surface of the substrate on two sides of the first conductive film (Fig. 12; col. 16, ln. 53-64).

In reference to claim 41, the isolation structure comprises a field shield isolation structure (16) in which a field shield electrode (polysilicon layer 16) is embedded (col. 14, ln. 60-col. 15, ln. 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 35 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld et al. in view of Tseng.

Schoenfeld discloses that the mask pattern is formed so that the second opening (140) in the mask is positioned above the element active region (Fig. 2). Schoenfeld does not specifically disclose planarizing the first conductive layer. Tseng discloses a method of manufacturing a DRAM in which the first conductive layer (11a) is planarized prior to photolithographically etching the layer to form the storage node of the capacitor (col. 4, ln. 59-62). It is well known in the art that planarizing layers which are to be subjected to photolithographic etching allows for the photoresist mask pattern to be more accurately etched. Schoenfeld, like Tseng, discloses a method of manufacturing a DRAM in which a first conductive layer (128) is subjected to photolithographic etching to form the storage node of a capacitor (col. 4, ln. 59-66). This etching process of the first conductive layer of Schoenfeld is required to be very precise in order to etch first openings in the conductive layer that extend all the way down to the insulating layer 126 while other openings are simultaneously etched which do not extend all the way down to the insulating layer (Fig. 3). At the time of the invention, it would have been obvious to one of ordinary skill in the art to planarize the first conductive layer of Schoenfeld as is done by Tseng because the etching of the first conductive layer is required to be very precise and, by planarizing the conductive layer before it is etched, the photoresist mask can be more accurately lithographically patterned, thereby providing a more precise etching of the first conductive layer.

2. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld et al. in view of Eaton, Jr. et al.

Schoenfeld discloses a method of forming a DRAM semiconductor device in which the element isolation regions (104) are formed by field oxidation (Fig. 1; col. 4, ln. 20-25). Eaton

also discloses a method of forming a DRAM structure. However, Eaton teaches that by using field shield isolation structures instead of field oxidation regions, the space between memory cells can be decreased, thereby decreasing the overall size of the semiconductor device (Fig. 3; col. 2, ln. 46-col. 3, ln. 42). Eaton also teaches that this decrease in the space between adjacent memory cells provides "a significant advantage" over the typical field oxidation process (col. 4, ln. 62-68). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the field shield isolation structures of Eaton for the field oxide regions of Schoenfeld because Eaton teaches that field shield isolation structures are superior to field oxidation regions for use in the DRAM manufacturing process because the field shield structures allow the space between adjacent memory cells to be decreased.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (703) 308-5840. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CLN
September 7, 2001

Carl Whitehead
CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800